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21 A reconfigurable arithmetic array for multimedia applications

Alan Marshall, Tony Stansfield, Igor Kostarnov, Jean Vuillemin, Brad Hutchings

February 1999 **Proceedings of the 1999 ACM/SIGDA seventh international symposium on Field programmable gate arrays**

Full text available: pdf(2.02 MB) Additional Information: full citation, references, citings, index terms

Keywords: 4-bit ALU, FPGA, multimedia, reconfigurable computing

22 Novel devices and approaches to programmable devices: A magnetoelectronic macrocell employing reconfigurable threshold logic

Steve P. Ferrera, Nicholas P. Carter

February 2004 **Proceeding of the 2004 ACM/SIGDA 12th international symposium on Field programmable gate arrays**

Full text available: pdf(288.34 KB) Additional Information: full citation, abstract, references, index terms

In this paper, we introduce a reconfigurable fabric based around a new class of circuit element: the hybrid Hall effect (HHE) magnetoelectronic device. Because they incorporate a ferromagnetic element, HHE devices are inherently non-volatile, retaining their state without a power supply. In addition, HHE devices are extremely well-suited to implementing threshold logic circuits, which allows many complex logic functions to be implemented in fewer gates than are required in systems based on AND-O ...

Keywords: PLA/CPLD, lookup table, magnetoelectronic circuits, non-volatility, threshold logic, wired-and logic

23 Poster session: Reconfigurable randomized K-way graph partitioning

Fatih Kocan

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(167.95 KB) Additional Information: full citation, abstract

In this paper, a randomized k-way graph partitioning algorithm is mapped onto reconfigurable hardware. The randomized algorithm relies on repetitive running of the same algorithm with different random number sequences to achieve the (near-)optimal solution. The run-time and hardware requirements of this reconfigurable solution per a random number sequence are O(|V|-K) cycles and O(|V|log|V|+|E|) gates and flip-flops, respectively. Performance is improved further at the expense of more hardware b ...

24 PipeRench: a co/processor for streaming multimedia acceleration

Seth Copen Goldstein, Herman Schmit, Matthew Moe, Mihai Budiu, Srihari Cadambi, R. Reed Taylor, Ronald Laufer

May 1999 **ACM SIGARCH Computer Architecture News , Proceedings of the 26th annual international symposium on Computer architecture**, Volume 27 Issue 2

Full text available: Additional Information:

full citation, abstract, references, citings, index terms

pdf(203.92 KB) Publisher Site

Future computing workloads will emphasize an architecture's ability to perform relatively simple calculations on massive quantities of mixed-width data. This paper describes a novel reconfigurable fabric architecture, PipeRench, optimized to accelerate these types of computations. PipeRench enables fast, robust compilers, supports forward compatibility, and virtualizes configurations, thus removing the fixed size constraint present in other fabrics. For the first time we explore how the bit-widt ...

25 Memory hierarchy reconfiguration for energy and performance in general-purpose processor architectures

Rajeev Balasubramonian, David Albonesi, Alper Buyuktosunoglu, Sandhya Dwarkadas

December 2000 **Proceedings of the 33rd annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(155.56 KB) ps(663.39 KB) Publisher Site

Additional Information: full citation, references, citings, index terms

26 Power-efficient layered turbo decoder processor

J. Dielissen, J. van Meerbergen, M. Bekooij, F. Harmsze, S. Sawitzki, J. Huisken, A. van der Werf

March 2001 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(62.48 KB) Additional Information: full citation, references, index terms

27 Interval scripts: a programming paradigm for interactive environments and agents

Claudio S. Pinhanez, Aaron F. Bobick

May 2003 **Personal and Ubiquitous Computing**, Volume 7 Issue 1

Full text available: pdf(1.08 MB) Additional Information: full citation, abstract, index terms

In this paper we present *interval scripts*, a new paradigm for the programming of interactive environments and computer characters. In this paradigm, actions and states of the users and the system computational agents are associated with temporal intervals. Programming is accomplished by establishing temporal relationships as constraints between the intervals. Unlike previous temporal constraint-based programming languages, we employ a strong temporal algebra based in Allen's interva ...

Keywords: Interactive spaces, Programming paradigms, Programming with constraints, System architecture, Temporal reasoning, Ubiquitous computing

28 DiscoTect: A System for Discovering Architectures from Running Systems

May 2004 **Proceedings of the 26th International Conference on Software Engineering**

Full text available: pdf(268.92 KB) Publisher Site

Additional Information: full citation, abstract

One of the challenging problems for software developersis guaranteeing that a system as built is consistentwith its architectural design. In this paper we describe atechnique that uses run time observations about an executingsystem to construct an architectural view of thesystem. With this technique we develop mappings thatexploit regularities in system implementation and architecturalstyle. These mappings describe how low-levelsystem events can be interpreted as more abstract architecturalopera ...

29 Simple, state-based approaches to program-based anomaly detection

C. C. Michael, Anup Ghosh

August 2002 **ACM Transactions on Information and System Security (TISSEC)**, Volume 5 Issue 3

Full text available: pdf(459.57 KB) Additional Information: full citation, abstract, references, citings, index terms

This article describes variants of two state-based intrusion detection algorithms from Michael and Ghosh [2000] and Ghosh et al. [2000], and gives experimental results on their performance. The algorithms detect anomalies in execution audit data. One is a simply constructed finite-state machine, and the other two monitor statistical deviations from normal program behavior. The performance of these algorithms is evaluated as a function of the amount of available training data, and they are compar ...

Keywords: Anomaly detection, finite automata, information system security, intrusion detection, machine

learning

30 Visualization using timelines
Gerald M. Karam
August 1994 **Proceedings of the 1994 ACM SIGSOFT international symposium on Software testing and analysis**
Full text available: pdf(1.45 MB) Additional Information: full citation, abstract, references, citings, index terms

A timeline is a linear, graphical visualization of events over time. For example, in concurrent application, events would represent state changes for some system object (such as a task or variable). A timeline display generator creates the graphical visualization from some record of events. This paper reports on a model for timeline display generators based on a formal model of event history and the objectives of timeline visualization. In this model, any timeline display generator is compl ...

31 Session 10B: VLIW exploration and deisgn synthesis: Synthesis of operation-centric hardware descriptions
James C. Hoe, Arvind
November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(117.64 KB) Additional Information: full citation, abstract, references, citings

Most hardware description frameworks, whether schematic or textual, use cooperating finite state machines (CFSM) as the underlying abstraction. In the CFSM framework, a designer explicitly manages the concurrency by scheduling the exact cycle-by-cycle interactions between multiple concurrent state machines. Design mistakes are common in coordinating interactions between two state machines because transitions in different state machines are not semantically coupled. It is also difficult to modify ...

32 Modeling for text compression
Timothy Bell, Ian H. Witten, John G. Cleary
December 1989 **ACM Computing Surveys (CSUR)**, Volume 21 Issue 4
Full text available: pdf(3.54 MB) Additional Information: full citation, abstract, references, citings, index terms, review

The best schemes for text compression use large models to help them predict which characters will come next. The actual next characters are coded with respect to the prediction, resulting in compression of information. Models are best formed adaptively, based on the text seen so far. This paper surveys successful strategies for adaptive modeling that are suitable for use in practical text compression systems. The strategies fall into three main classes: finite-context modeling, i ...

33 Low power DSP's for wireless communications (embedded tutorial session)
Ingrid Verbauwhede, Chris Nicol
August 2000 **Proceedings of the 2000 international symposium on Low power electronics and design**
Full text available: pdf(424.32 KB) Additional Information: full citation, abstract, references, citings, index terms

Wireless communications and more specifically, the fast growing penetration of cellular phones and cellular infrastructure are the major drivers for the development of new programmable Digital Signal Processors (DSPs). In this tutorial, an overview will be given of recent developments in DSP processor architectures, that makes them well suited to execute computationally intensive algorithms typically found in communications systems. DSP processors have adapted instruction sets, memory archi ...

Keywords: architectures, digital signal processing, programmable processors, wireless communications

34 Operational characteristics of a harware-based pattern matcher
Roger L. Haskin, Lee A. Hollaar
March 1983 **ACM Transactions on Database Systems (TODS)**, Volume 8 Issue 1
Full text available: pdf(1.84 MB) Additional Information: full citation, abstract, references, citings, index terms

The design and operation of a new class of hardware-based pattern matchers, such as would be used in a backended database processor in a full-text or other retrieval system, is presented. This recognizer is based on a unique implementation technique for finite state automata consisting of partitioning the state table among a number of simple digital machines. It avoids the problems generally associated with implementing finite state machines, such as large state table memories, complex cont ...

Keywords: backend processors, computer system architecture, finite state automata, full text retrieval systems, text searching

35 DPGA utilization and application
André DeHon
February 1996 **Proceedings of the 1996 ACM fourth international symposium on Field-programmable gate arrays**
Full text available: pdf(120.20 KB) Additional Information: full citation, references, citings, index terms

36 Dynamic translation: Retargetable and reconfigurable software dynamic translation
K. Scott, N. Kumar, S. Velusamy, B. Childers, J. W. Davidson, M. L. Soffa
March 2003 **Proceedings of the international symposium on Code generation and optimization: feedback-directed and runtime optimization**
Full text available: pdf(1.14 MB) Publisher Site Additional Information: full citation, abstract, references, index terms

Software dynamic translation (SDT) is a technology that permits the modification of an executing program's instructions. In recent years, SDT has received increased attention, from both industry and academia, as a feasible and effective approach to solving a variety of significant problems. Despite this increased attention, the task of initiating a new project in software dynamic translation remains a difficult one. To address this concern, and in particular, to promote the adoption of SDT techn ...

37 Poster session: FPGAs in critical hardware/software systems
Adrian J. Hilton J. Adrian J. Hilton, Gemma Townson, Jon G. Hall
February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**
Full text available: pdf(187.99 KB) Additional Information: full citation, abstract

FPGAs are being used in increasingly complex roles in critical systems, interacting with conventional critical software. Established safety standards require rigorous justification of safety and correctness of the conventional software in such systems. Newer standards now make similar requirements for safety-related electronic hardware, such as FPGAs, in these systems. In this paper we examine the current state-of-the-art in programming FPGAs, and their use in conventional (low-criticality) hard ...

38 Improving Compression Ratio, Area Overhead, and Test Application Time for System-on-a-Chip Test Data Compression/Decompression
P. Gonciari, B. Al-Hashimi, N. Nicolici
March 2002 **Proceedings of the conference on Design, automation and test in Europe**
Full text available: pdf(192.88 KB) Publisher Site Additional Information: full citation, abstract

This paper proposes a new test data compression/decompression method for systems-on-a-chip. Themethod is based on analyzing the factors that influencetest parameters: compression ratio, area overhead and testapplication time. To improve compression ratio, the newmethod is based on a Variable-length Input Huffman Coding(VIHC), which fully exploits the type and length of the patterns,as well as a novel mapping and reordering algorithmproposed in a pre-processing step. The new VIHC algorithmis comb ...

39 Poster session: An estimation and exploration methodology from system-level specifications: application to FPGAs
Sebastien Bilavarn, Guy Gogniat, Jean Luc Philippe
February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**
Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

Rapid evaluation and design space exploration from early specifications are important issues in the design cycle. We propose an original area vs. delay estimation methodology that targets reconfigurable architectures. Two main steps compose the estimation flow: i) structural estimations where architectural solutions are defined at the RT level, this step is technological independent and performs an automatic design space exploration and ii) physical estimations which perform technology mapping t ...

40 Automating process discovery through event-data analysis
Jonathan E. Cook, Alexander L. Wolf
April 1995 **Proceedings of the 17th international conference on Software engineering**
Full text available: Additional Information:

pdf(1.04 MB) full citation, references, abstract, index terms

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1 Special session on reconfigurable computing: Reconfigurable platforms for ubiquitous computing

Manfred Glesner, Thomas Hollstein, Leandro Soares Indrusiak, Peter Zipf, Thilo Pionteck, Mihail Petrov, Heiko Zimmer, Tudor Murgan

April 2004 **Proceedings of the first conference on computing frontiers on Computing frontiers**

Full text available: pdf(479.97 KB) Additional Information: full citation, abstract, references, index terms

Ubiquitous computing requires flexibilty. Melting distributed electronic devices into everyday's life implies the need to adapt to evolving standards and dynamic environments. Furthermore, to gain user acceptance, such devices should be able to adapt to different usage patterns and user profiles. Scalability is also an important issue, allowing functional enhancements to already deployed systems. In this work we address these issues applying the concept of reconfigurability on different abstract ...

Keywords: communication, dynamic power management, networks-on-chip, reconfigurable hardware, reconfigurable processors, reconfiguration, ubiquitous computing

2 Exploiting ILP in page-based intelligent memory

Mark Oskin, Justin Hensley, Diana Keen, Frederic T. Chong, Matthew Farrens, Aneet Chopra

November 1999 **Proceedings of the 32nd annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(1.35 MB) Publisher Site Additional Information: full citation, abstract, references, index terms

This study compares the speed, area, and power of different implementations of Active Pages [OCS98], an intelligent memory system which helps bridge the growing gap between processor and memory performance by associating simple functions with each page of data. Previous investigations have shown up to 1000X speedups using a block of reconfigurable logic to implement these functions next to each sub-array on a DRAM chip. In this study, we show that instruction-level parallelism, n ...

3 Balancing performance and flexibility with hardware support for network architectures

Ilija Hadžić, Jonathan M. Smith

November 2003 **ACM Transactions on Computer Systems (TOCS)**, Volume 21 Issue 4

Full text available: pdf(712.93 KB) Additional Information: full citation, abstract, references, index terms

The goals of performance and flexibility are often at odds in the design of network systems. The tension is common enough to justify an architectural solution, rather than a set of context-specific solutions. The Programmable Protocol Processing Pipeline (P4) design uses programmable hardware to selectively accelerate protocol processing functions. A set of field-programmable gate arrays (FPGAs) and an associated library of network processing modules implemented in hardware are augmented with so ...

Keywords: FPGA, P4, computer networking, flexibility, hardware, performance, programmable logic devices, programmable networks, protocol processing

4 Discovering models of software processes from event-based data

Jonathan E. Cook, Alexander L. Wolf

July 1998 **ACM Transactions on Software Engineering and Methodology (TOSEM)**, Volume 7 Issue 3

Full text available: pdf(369.76 KB) Additional Information: full citation, abstract, references, citings, index terms, review

Many software process methods and tools presuppose the existence of a formal model of a process. Unfortunately, developing a formal model for an on-going, complex process can be difficult, costly, and error prone. This presents a practical barrier to the adoption of process technologies, which would be lowered by automated assistance in creating formal models. To this end, we have developed a data analysis technique that we term process discovery. Under this technique, data ...

Keywords: Balboa, process discovery, software process, tools

5 The Parallel Protocol Engine
Matthias Kaiserswerth
December 1993 **IEEE/ACM Transactions on Networking (TON)**, Volume 1 Issue 6

Full text available: pdf(1.65 MB) Additional Information: full citation, references, citings, index terms, review

6 Realizing OpenGL: two implementations of one architecture
Mark J. Kilgard
August 1997 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**

Full text available: pdf(1.66 MB) Additional Information: full citation, references, citings, index terms

Keywords: O2, OpenGL, graphics hardware architecture, infinite-reality

7 PipeRench implementation of the instruction path coprocessor
Yuan Chou, Pazhani Pillai, Herman Schmit, John Paul Shen
December 2000 **Proceedings of the 33rd annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(238.33 KB) ps(2.67 MB) Publisher Site Additional Information: full citation, references, citings, index terms

8 Security on FPGAs: State-of-the-art implementations and attacks
Thomas Wollinger, Jorge Guajardo, Christof Paar
August 2004 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 3 Issue 3

Full text available: pdf(298.73 KB) Additional Information: full citation, abstract, references, index terms

In the last decade, it has become apparent that embedded systems are integral parts of our every day lives. The wireless nature of many embedded applications as well as their omnipresence has made the need for security and privacy preserving mechanisms particularly important. Thus, as field programmable gate arrays (FPGAs) become integral parts of embedded systems, it is imperative to consider their security as a whole. This contribution provides a state-of-the-art description of security issues ...

Keywords: Cryptography, FPGA, attacks, cryptographic applications, reconfigurable hardware, reverse engineering, security

9 Attacking the semantic gap between application programming languages and configurable hardware
Greg Snider, Barry Shackleford, Richard J. Carter
February 2001 **Proceedings of the 2001 ACM/SIGDA ninth international symposium on Field programmable gate arrays**

Full text available: pdf(256.55 KB) Additional Information: full citation, abstract, references, index terms

It is difficult to exploit the massive, fine-grained parallelism of configurable hardware with a conventional application programming language such as C, Pascal or Java. The difficulty arises from the mismatch between the synchronous, concurrent processing capability of the hardware and the expressiveness of the language-the so-called "semantic gap." We attack this problem by using a programming model matched to the hardware's capabilities that can be implemented in any (unmodified) objec ...

10 Pipelined architectures: MaRS: a macro-pipelined reconfigurable system

Nozar Tabrizi, Nader Bagherzadeh, Amir H. Kamalizad, Haitao Du
April 2004 **Proceedings of the first conference on computing frontiers on Computing frontiers**

Full text available: pdf(193.48 KB) Additional Information: full citation, abstract, references, index terms

We introduce MaRS, a reconfigurable, parallel computing engine with special emphasis on scalability, lending itself to the computation-/data-intensive multimedia data processing and wireless communication. Global communication between the processing elements (PEs) in MaRS is performed through a 2D-mesh deadlock-free network, avoiding any concerns due to non-scalable bus-based communication. Additionally, we have developed a second layer of inter-PE connection realized by distributed shared regis ...

Keywords: 2D-mesh network, MIMD, computer graphics, multimedia, reconfigurable architectures, wireless communication

11 The design of dynamically reconfigurable datapath coprocessors
Zhining Huang, Sharad Malik, Nahri Moreano, Guido Araujo
May 2004 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 3 Issue 2

Full text available: pdf(467.82 KB) Additional Information: full citation, abstract, references, index terms

Increasing nonrecurring engineering and mask costs are making it harder to turn to hardwired application specific integrated circuit (ASIC) solutions for high-performance applications. The volume required to amortize these high costs has been increasing, making it increasingly expensive to afford ASIC solutions for medium-volume products. This has led to designers seeking programmable solutions of varying sorts using these so-called programmable platforms. These programmable platforms span a lar ...

Keywords: Loop pipelining, coarse-grain reconfigurable fabric, datapath synthesis, interconnection design, reconfigurable datapath

12 Special session on reconfigurable computing: The happy marriage of architecture and application in next-generation reconfigurable systems
Ingrid Verbauwhede, Patrick Schaumont
April 2004 **Proceedings of the first conference on computing frontiers on Computing frontiers**

Full text available: pdf(388.28 KB) Additional Information: full citation, abstract, references, index terms

New applications and standards are first conceived only for functional correctness and without concerns for the target architecture. The next challenge is to map them onto an architecture. Embedding such applications in a portable, low-energy context is the art of molding it onto an energy-efficient target architecture combined with an energy efficient execution. With a reconfigurable architecture, this task becomes a two-way process where the architecture adapts to the application and vice-vers ...

Keywords: embedded, real-time systems

13 System-level power optimization: techniques and tools
Luca Benini, Giovanni de Micheli
April 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 2

Full text available: pdf(365.22 KB) Additional Information: full citation, abstract, references, citings, index terms

This tutorial surveys design methods for energy-efficient system-level design. We consider electronic sytems consisting of a hardware platform and software layers. We consider the three major constituents of hardware that consume energy, namely computation, communication, and storage units, and we review methods of reducing their energy consumption. We also study models for analyzing the energy cost of software, and methods for energy-efficient software design and compilation. This survery ...

14 A decade of reconfigurable computing: a visionary retrospective
R. Hartenstein
March 2001 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(768.60 KB) Additional Information: full citation, references, citings, index terms

15 Software for Reconfigurable Systems: Performance-constrained pipelining of software loops onto reconfigurable hardware
Greg Snider

February 2002 **Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays**

Full text available: pdf(206.27 KB) Additional Information: full citation, abstract, references, citings

Retiming and slowdown are algorithms that can be used to pipeline synchronous circuits. *Iterative modulo scheduling* is an algorithm for software pipelining in the presence of resource constraints. Integrating the best features of both yields a pipelining algorithm, *retimed modulo scheduling*, that can more effectively exploit the idiosyncrasies of reconfigurable hardware. It also fits naturally into a design space exploration process to trade-off speed for power, energy or ar ...

16 Dynamically reconfiguring multimedia components: a model-based approach

Scott Mitchell, Hani Naguib, George Coulouris, Tim Kindberg

September 1998 **Proceedings of the 8th ACM SIGOPS European workshop on Support for composing distributed applications**

Full text available: pdf(342.50 KB) Additional Information: full citation, index terms

17 String matching on multicontext FPGAs using self-reconfiguration

Reetinder P. S. Sidhu, Alessandro Mei, Viktor K. Prasanna

February 1999 **Proceedings of the 1999 ACM/SIGDA seventh international symposium on Field programmable gate arrays**

Full text available: pdf(1.10 MB) Additional Information: full citation, references, citings, index terms

18 Testing TAPed cores and wrapped cores with the same test access mechanism

M. Benabdenbi, W. Maroufi, M. Marzouki

March 2001 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(106.84 KB) Additional Information: full citation, references, index terms

19 Poster session: On hiding latency in reconfigurable systems: the case of merge-sort for an FPGA-based system

Hossam ElGindy, George Ferizis

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(197.05 KB) Additional Information: full citation, abstract

Recursive solutions are effective software techniques that are difficult to map into hardware due to their dependency on input size and data values. As a result, most high-level design tools do not allow for recursive calls. In this paper we present a technique for mapping the merge-sort algorithm, as a case study, into a reconfigurable system. Our mapping employs an on-line prediction method to reconfigure the necessary hardware only when the need arises, and to hide the reconfiguration delay. ...

20 Poster session: A high-speed successive erasure BCH decoder architecture

Thomas Buerner

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(197.05 KB) Additional Information: full citation, abstract

A new high speed architecture for a BCH successive erasure decoder is presented. The Berlekamp-Massey based decoder by Sarwate and Shanbhag is extended to handle successive erasures. The critical path in the calculation submodules is increased from Tadd+Tmult to Tadd+Tmult+Tmux. The proposed architecture is implemented exemplary for a BCH(63,45,7) code with up to two erasures on a XILINX Spartan2E300-7. Thus a clock frequency of 95 MHz is reached using 47% of the available slices instead of 105 ...

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